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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,515	08/31/2001	Samuel H. Duncan	15311-2292	3331

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EXAMINER	
MASON, DONNA K	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,515	DUNCAN ET AL.	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed January 13, 2005 have been fully considered but they are not persuasive.

Pawlowski in view of PCI Specification

Regarding the rejection of claims 1-9 and 11-18 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,956,516 to Pawlowski in view of *PCI Local Bus Specification Product Version*, Rev. 2.1 ("*PCI Specification*"), Applicant argues that Pawlowski in view of the *PCI Specification* fails to teach or suggest all the features of independent claims 1 and 12. More specifically, Applicant argues that Pawlowski fails to teach the limitation, "in response to the interrupt being serviced, generating a first ordered message, the first ordered message notifying the subject I/O device that the interrupt has been serviced", as claimed.

However, the Examiner is not persuaded that Pawlowski fails to teach this feature. Contrary to Applicant's arguments (*see* pages 9-10), the Examiner does not equate Pawlowski's "interrupt message" with the claimed "first ordered message". Instead, the Examiner equates Pawlowki's "IRR bit" (*see* column 6, lines 40-41) with the claimed "first message", and cites the *PCI Specification* for teaching an "ordered message." As described in Pawlowski, the IRR bit is set when the interrupt has been serviced, thus providing a first message notifying the subject I/O device that the interrupt has been serviced, as claimed.

Therefore, the Examiner cannot allow claims 1-9 and 11-18.

Bashford in view of PCI Specification

Regarding the rejection of claims 1, 12 and 15 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,629,179 to Bashford in view of *PCI Local Bus Specification Product Version*, Rev. 2.1 ("*PCI Specification*"), Applicant argues that Bashford in view of the *PCI Specification* fails to teach or suggest all the features of independent claims 1 and 12. More specifically, Applicant argues that Bashford fails to teach the limitation, "in response to the interrupt being serviced, generating a first ordered message, the first ordered message notifying the subject I/O device that the interrupt has been serviced", as claimed.

However, the Examiner is not persuaded that Bashford fails to teach this feature. Contrary to Applicant's arguments (*see* pages 10-12), the Examiner does not equate Bashford's "message signaled interrupt" with the claimed "first ordered message". Instead, the Examiner equates Bashford's "sent signal" (*see* column 9, lines 50-64) with the claimed "first message", and cites the *PCI Specification* for teaching an "ordered message." As described in Bashford, the sent signal is sent when the interrupt has been serviced, thus providing a first message notifying the subject I/O device that the interrupt has been serviced, as claimed.

Therefore, the Examiner cannot allow claims 1, 12 and 15.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 and 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,956,516 to Pawlowski in view of *PCI Local Bus Specification Product Version*, Rev. 2.1 ("*PCI Specification*").

With regard to claims 1-8, Pawlowski discloses a method for preventing passive release of interrupts within a computer system, the computer system having at least one processor (Fig. 1, item 12) for servicing the interrupts, one or more input/output (I/O) devices (Fig. 1, items 50, 52, 54, 56, and 58) configured to issue interrupts (column 3, lines 24-26), and an I/O bridge (Fig. 1, item 16) having a plurality of ports (Fig. 1, item 38) to which I/O devices are coupled and configured to interface between the I/O devices and the processor. The method includes the steps of: asserting an interrupt signal by a subject I/O device coupled to a given port of the I/O bridge (column 3, lines 24-26); forwarding an interrupt message corresponding to the interrupt signal to the processor for servicing (column 3, lines 50-53); setting an interrupt pending flag in response to assertion of the interrupt signal (column 5, lines 45-49). In response to the interrupt being serviced, generating a first message, the first message notifying the subject I/O device that the interrupt has been serviced, and sending the first message to the given port of the I/O bridge (column 6, lines 40-41); generating a second message for clearing the interrupt pending flag, and sending the second message to the given port of the I/O bridge after the first message has been sent (column 6, lines 44-45); deasserting the interrupt signal in response to the first message (column 6, lines 49-50);

and clearing the interrupt pending flag at the interrupt file in response to the second message (column 6, lines 40-41). With regard to the features of claims 2-8, see column 6, lines 37-65.

With regard to claim 9, Pawlowski discloses the method where the computer system includes a plurality of processors (column 3, lines 50-53), at least one of which is designated to service interrupts from the subject I/O device, and a plurality of I/O bridges (Fig. 1, items 16 and 82) each I/O bridge coupled to a plurality of I/O devices configured to assert respective interrupt signals.

With regard to claims 11 and 18, Pawlowski discloses the method and computer system where the interrupt signals are level sensitive interrupts (LSIs) (column 6, lines 21-36).

With regard to claim 12, Pawlowski discloses a computer system (Fig. 1, item 10) including: a plurality of input/output (I/O) devices (Fig. 1, items 50, 52, 54, 56, and 58) configured to assert and deassert respective interrupt signals (column 3, lines 24-26); at least one processor (Fig. 1, item 12) for servicing interrupts from the I/O devices; and an I/O bridge (Fig. 1, item 16) configured to interface between the I/O devices and the at least one processor, the I/O bridge having a plurality of ports (Fig. 1, item 38) to which the I/O devices are coupled and an interrupt controller (Fig. 1, item 34) configured to detect the assertion and deassertion of the interrupt signals. The interrupt controller, in response to assertion of an interrupt signal by a subject I/O device coupled to a given I/O bridge port, issues an interrupt message to the processor and sets an interrupt pending flag (column 5, lines 45-49). The processor, upon servicing the interrupt, sends

first and second messages to the given port of the I/O bridge, the first message notifying the subject I/O device that the interrupt has been serviced, and the second message clearing the interrupt pending flag (column 6, lines 37-48); the subject I/O device deasserts the interrupt signal in response to the first message (column 6, lines 49-50); and the interrupt pending flag is cleared in response to the second message (column 6, lines 40-41).

With regard to claims 13 and 14, Pawlowski discloses the computer system where the I/O bridge further includes an interrupt port (Fig. 1, item 38) at which the interrupt controller is disposed, and the given port of the I/O bridge forwards the second message to the interrupt port after forwarding the first message to the subject I/O device. Pawlowski also discloses the computer system where the interrupt port of the I/O bridge includes at least one register (Fig. 3, item 170) at which the interrupt pending flag is implemented.

With regard to claim 15, Pawlowski discloses the computer system where the I/O bridge port includes a read cache for buffering messages received from the at least one processor, and an ordering engine operatively coupled to a read cache, and the ordering engine is configured to release messages buffered in the read cache in the same order as which they were received (column 4, lines 56-60).

With regard to claims 16 and 17, Pawlowski discloses computer system, further including an interrupt collector having a parallel-load shift register for receiving the interrupt signals from the I/O devices, the serial shift register configured to transfer information indicating the assertion or deassertion of interrupt signals to the interrupt

controller through one or more serial shift operations, and where the interrupt collector transfers the information in response to a request from the interrupt controller, and the interrupt controller is configured to limit the number of serial shift operations performed by the interrupt collector so as to receive only information associated with interrupt signals that have been enabled (*see* column 5, lines 41-64).

Pawlowski does not expressly disclose where the first message and second message are each an ordered message, as claimed.

The *PCI Specification* discloses ordered messages (page 258, section entitled "Producer - Consumer Ordering Model").

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the *PCI Specification* with Pawlowski. The suggestion or motivation for doing so would have been to prevent deadlock of the system bus (page 257).

Therefore, it would have been obvious to combine the *PCI Specification* with Pawlowski to obtain the invention as specified in claims 1-9 and 11-18.

4. Claims 1, 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,629,179 to Bashford.

With regard to claims 1 and 12, Bashford discloses a method and computer system (Fig. 1) including: a plurality of input/output (I/O) devices (Fig. 1, items 116) configured to assert and deassert respective interrupt signals; at least one processor (Fig. 1, item 106) for servicing interrupts from the I/O devices; and an I/O bridge (Fig. 1,

item 112) configured to interface between the I/O devices and the at least one processor, the I/O bridge having a plurality of ports (Fig. 2, item 206) to which the I/O devices are coupled and an interrupt controller (Fig. 2, item 210 and Fig. 4, item 402) configured to detect the assertion and deassertion of the interrupt signals. The interrupt controller, in response to assertion of an interrupt signal by a subject I/O device coupled to a given I/O bridge port, issues an interrupt message to the processor and sets an interrupt pending flag (column 6, lines 57-67 to column 7, lines 1-41). The processor, upon servicing the interrupt, sends first and second messages to the given port of the I/O bridge, the first message notifying the subject I/O device that the interrupt has been serviced, and the second message clearing the interrupt pending flag (column 9, lines 50-64); the subject I/O device deasserts the interrupt signal in response to the first message (column 9, lines 50-64); and the interrupt pending flag is cleared in response to the second message (column 9, lines 50-64).

With regard to claim 15, Bashford discloses the computer system where the I/O bridge port includes a read cache for buffering messages received from the at least one processor, and an ordering engine operatively coupled to a read cache, and the ordering engine is configured to release messages buffered in the read cache in the same order as which they were received (*see generally*, Fig. 4 and column 2, lines 40-67 to column 3, lines 1-50).

Bashford does not expressly disclose where the first message and second message are each an ordered message, as claimed.

The *PCI Specification* discloses ordered messages (page 258, section entitled "Producer - Consumer Ordering Model").

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the *PCI Specification* with Bashford. The suggestion or motivation for doing so would have been to prevent deadlock of the system bus (page 257).

Therefore, it would have been obvious to combine the *PCI Specification* with Bashford to obtain the invention as specified in claims 1, 12, and 15.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM